## REMARKS

Claims 1-8 are pending and under consideration.

In the Office Action of March 17, 2008, claims 1, 2 and 8 were rejected as anticipated by Arima (JP 05-265767), Claim 3 was rejected as obvious in view of Arima and Hashimoto (JP57-071508), claims 4 and 5 were rejected as obvious in view of Arima and Dawson et al (USP 6311213), and claim 6 was rejected as obvious in view of Arima, Dawson et al and Kim (USP 6587915). These rejections are traversed.

Additionally, a correction to the specification was requested. The correction has been made.

Claims 1-4, 6 and 8 have been amended as to form and to clarify same. No amendment was made in response to the rejection. No new matter was added.

Regarding the rejections of the claims, all of the rejections are based on the comparison of the use of a CPU in Arima with the read control circuit of the claims. This is an improper comparison.

In that regard, the claims require that a read control circuit, which is different than the CPU, perform the recited determination as to whether a data block is faulty or not. The CPU is provided with the boot program instructions only after the read control circuit has made a determination that the data block read out is not faulty.

In Arima, the CPU executes a program that causes the CPU to do the fault checking. This is not even remotely the same as having the fault checking done by a completely different circuit, namely the recited read control circuit.

Further, in Arima, the CPU must decide "whether the program code is normal," and a program for deciding "whether the program code is normal" must be invoked. It is presupposed that the invoked program is in a ROM and that the invoked program code is absolutely free of any error. After all, in order for the CPU to do something, a storage region in which program codes without error is a necessity.

This is not the same as deciding whether a data block is faulty. The fault could arise because of bad blocks in the memory.

As explained in the published specification:

Conventionally, it has been a problem to ensure that a NAND type flash memory has not any specific bad block because the cost of the test that needs to be conducted for that purpose before shipment is enormous and the yield of manufacturing such flash memories is inevitably reduced by the test. However, according to the invention, it is possible to use a low cost high capacity flash memory as boot device if bad blocks randomly exist therein. Thus, it is possible to constantly stably start such a memory while suppressing the cost of manufacturing the entire semiconductor device.

US Pub. 2008/0046637, Paragraph [0056].

Regarding the other references, similarly a CPU invokes a program to determine whether program codes are abnormal. But, again, in the presently claimed invention, the CPU is not involved in this determination. Instead, the determination is made by the read control circuit.

Accordingly, it is submitted that Arima does not support the rejection of any claim and all claims are patentable over the cited references, regardless of what they might teach. Notice to that effect is requested.

Respectfully submitted,

Dated: July 2, 2008 By: /David R. Metzger/

David R. Metzger
Registration No. 32,919
SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(312) 876-8000